Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented ~~each time an operation is executed~~ in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation,

wherein the state unit includes an electrical capacitor; and wherein the state is a charge state of the electrical capacitor.

Claim 2 (original). Processor according to claim 1, wherein the state unit has continuous states.

Claim 3 (original). Processor according to claim 1, wherein the state unit is so designed that the state of the state unit is also a function of time.

Claim 4 (original). Processor according to claim 1, wherein the state unit is so designed that, when the computation unit performs no operations, the state of the state unit changes in a direction which is opposite to the direction of change in response to execution of an operation.

Claim 5 (original). Processor according to claim 1, wherein the state unit is so designed that the speed of the computation unit is inversely proportional to the variable, by which the state of the state unit can be represented.

Claim 6 (original). Processor according to claim 1, wherein the state unit is so designed that the speed of the computation unit is inversely exponential to the variable, by which the state of the state unit can be represented.

Claims 7-9 (canceled).

Claim 10 (original). Processor according to claim 1, wherein a frequency of a clock rate of the computation unit can be controlled according to the state of the state unit.

Claim 11 (original). Processor according to claim 1, wherein a number of bits which are processed by an operation in the computation unit can be controlled according to the state of the state unit.

Claim 12 (original). Processor according to claim 1, wherein the operation is a cryptographic operation for encrypting or decrypting information.

Claim 13 (currently amended). Method for executing an operation in a processor at a variable speed, comprising the following steps:

increasing a variable which represents a state of a state unit by a specified value in response to the execution of an operation ~~each time the operation is executed~~ by a computation unit of the processor; and

decreasing the speed of the computation unit in response to the increase of the variable due to the execution of the operation,

wherein the variable is a charge of an electrical capacitor.

Claim 14 (new). Processor according to claim 1, wherein the processor comprises a clock generator;

wherein the clock generator is adapted such that the greater the charge of the electrical capacitor is, the lower is a frequency of a clock signal generated by the clock generator; and

wherein the frequency of the clock signal influences the speed of the computation unit.

Claim 15 (new). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation,

wherein the state unit includes a unit with a thermal capacitance;

wherein the state is a temperature of the unit;

wherein the unit with a thermal capacitance also has a second temperature; and

wherein the speed of the computation unit is also controlled according to the second temperature.

Claim 16 (new). The processor according to claim 15, wherein the speed of the computation is controlled in response to a difference signal representing a difference between the first temperature and the second temperature.

Claim 17 (new). The processor according to claim 15, wherein the processor comprises a first temperature sensor adapted to determine the first temperature and a second temperature sensor adapted to determine the second temperature,

wherein the first temperature sensor and the second temperature sensor are located at different places of the thermal capacitance.

Claim 18 (new). The processor according to claim 17, wherein the first temperature sensor and the second temperature sensor are located at two places of the computation unit which warm up to different extents or at different rates on execution of an operation by the computation unit.

Claim 19 (new). The processor according to claim 15, wherein the processor is adapted such that a difference between the first temperature and the second temperature results in a reduction of the speed of the computation unit.

Claim 20 (new). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation,

wherein the state unit includes a unit with a thermal capacitance; wherein the state is a temperature of the unit; and

wherein the processor comprises an electrical filament resistor adapted to supply energy to the thermal capacitance in response to the execution of an operation in the computation unit.

Claim 21 (new). Processor comprising:

a computation unit for executing an operation at a speed;

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation; and

a clock generator;

wherein the state unit includes a unit with a thermal capacitance;

wherein the state is a temperature of the unit;

wherein the state unit comprises a temperature sensor;

wherein the clock generator is adapted such that an output signal of the temperature sensor controls a clock rate generated by the clock generator; and

wherein the clock rate generated by the clock generator controls the speed of the computation unit.

Claim 22 (new). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation;

wherein the state unit is so designed that the speed of the computation unit is inversely proportional to the variable, by which the state of the state unit can be represented, or

wherein the state unit is so designed that the speed of the computation unit is inversely exponential to the variable, by which the state of the state unit can be represented.

Claim 23 (new). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation; and

a clock generator;

wherein the clock generator is adapted to change the speed of the computation unit in steps in dependence on the state of the state unit, to set the speed of the computation unit to a first high speed or to a second lower speed.

Claim 24 (new). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation;

wherein the processor is adapted allow for setting a factor for a relationship between a state of the state unit and a speed of the calculation unit or for setting an amount of energy supplied to the state unit by means of a programmable parameter.

Claim 25 (new). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation,

wherein a number of bits which are processed simultaneously by an operation in the computation unit is controlled according to the state of the state unit.

Claim 26 (new). Processor comprising:

a computation unit for executing an operation at a speed; and

a state unit, which has a state, wherein the speed of the computation unit is controllable according to the state of the state unit, wherein the state unit is designed to cause an increase of a variable by which the state of the state unit can be

represented in response to the execution of an operation by the computation unit, and to decrease the speed of the computation unit in response to the increase of the variable due to executing of the operation,

wherein wait clock intervals are introduced to decrease the speed of the calculation unit.